IN THE CLAIMS

Please amend the claims to read as follows:

1. (original): A circuit for delaying power interruption to a non-volatile memory device comprising:
a power supply having an output connected to the non-volatile memory device;
a charge-storing device connected to the output of the power supply; and,
a DC-to-DC converter connected at its input to the charge-storing device and the power supply and connected at its output to the non-volatile memory device such that upon interruption of the power supply, the charge-storing device provides sufficient input voltage to the DC-to-DC converter to provide rated output to the non-volatile memory device for a time sufficient for the non-volatile memory device to complete a write cycle.

2. (previously presented): A circuit as recited in claim 1 wherein the charge-storing device is a capacitor.

3. (previously presented): A circuit as recited in claim 1 wherein the charge-storing device is an electrolytic capacitor.

4. (previously presented): A circuit as recited in claim 1 wherein the charge-storing device is a super capacitor.

5. (previously presented): A circuit as recited in claim 1 wherein the charge-storing device comprises a plurality of capacitors connected in parallel.

6. (previously presented): A circuit as recited in claim 1 further comprising an inductor connected in parallel with the DC-to-DC converter.

7. (previously presented): A circuit as recited in claim 6 further comprising a diode connected in series between the inductor and the output of the DC-to-DC converter.

8. (previously presented): A circuit as recited in claim 1 further comprising a diode at the input of the charge storing device connected such that the flow of electric current from the charge-storing device to the power supply is prevented.

9. (canceled)

10. (original): A method of supplying power to a non-volatile memory device comprising:

providing regulated power from a power supply;

storing electrical charge from the power supply in a charge-storing device;

transferring the stored electrical charge upon interruption of the power supply to the input of a DC-to-DC converter at a potential sufficient to operate the DC-to-DC converter; and

supplying regulated DC power from the output of the DC-to-DC converter to the non-volatile memory device for a time sufficient for the non-volatile memory device to complete a full write cycle.

Claims 11 – 16 (canceled)

17. (original): A method of preventing data corruption in a non-volatile memory device comprising:

determining whether a control signal sent to the non-volatile memory device is a reset signal;

delaying the control signal if the control signal is a reset signal for time sufficient for the non-volatile memory device to complete a memory write cycle;

providing regulated power from a power supply to the non-volatile memory device;

storing electrical charge from the power supply in a charge-storing device;

transferring the stored electrical charge upon interruption of the power supply to the input of a DC-to-DC converter at a potential sufficient to operate the DC-to-DC converter; and

supplying regulated DC power from the output of the DC-to-DC converter to the non-volatile memory device for a time sufficient for the non-volatile memory device to complete a write cycle.

18. (original): A method as recited in claim 17 wherein the non-volatile memory device is a flash memory.

19. (original): A method as recited in claim 18 wherein the flash memory is a NAND-type flash memory.

20. (original): A circuit as recited in claim 1 wherein the non-volatile memory device is a NAND-type flash memory.